The Rating And Application of SCR's Designed for Switching at High Frequencies

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The Rating and Application of SCRs Designed for Power Switching at High Frequencies

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Abstract—**Inverter, chopper, and other pulse applications, operating at repetition rates up to 25 000 pps (pulses per second), are very demanding for the silicon controlled rectifier because of the high rates of rise of anode current (*di/dt*) which are imposed. The *di/dt* rating of the SCR is important since high *di/dt* of anode current produces excessive heating in the device and, if this is not controlled, device destruction will result. This necessitates an SCR specifically designed for such applications and, also, a family of performance curves to enable the circuit designer to determine its capability reliably in his particular application. These performance curves consider the combined effect of the important SCR dynamic parameters, *di/dt*, *dv/dt*, and turn-off time. As a result, the high-frequency SCR is adaptable to many applications which previously imposed dynamic conditions too severe for SCRs to withstand because of excessive switching losses. The use of these curves is demonstrated through actual circuit application examples. The rating methods used for high-frequency SCRs are discussed and compared to methods normally used for conventional SCRs which do not include the effects of switching losses and high *di/dt*.**

High-Frequency Performance Curves

THE HIGH-FREQUENCY performance curves represent new concepts in device characterization. The primary purpose of the curves is to provide the design engineer with information he can use directly to apply the high-frequency SCR to his circuit. Since most actual circuits impose the important SCR dynamic parameters on a cyclic basis, the SCR must be capable of operating under the stress of the combined effects of rate of rise of anode current (*di/dt*), turn-off time, and rate of rise of anode voltage (*dv/dt*). These effects are interdependent, and characterization of these parameters on an individual basis is not sufficient to ensure satisfactory operation of the SCR in the actual circuit. Therefore, the principle of concurrent characterization of the dynamic characteristics is necessary and has been employed in the development of the performance curves [1].

Peak Current Rating Curves

Figures 1, 2, and 3 show the current ratings of a high-frequency SCR as a function of sinusoidal pulse base width and frequency for three different values of SCR case temperature. These curves provide the basic device rating information needed by the circuit designer. Since concurrent characterization has been employed, all ratings apply for a specified minimum circuit turn-off time and a specified maximum circuit *dv/dt*.

These curves allow the circuit designer to predict SCR performance over a wide variety of operating conditions. The range of pulse repetition rates is 10 to 25 000 pps. Pulse base widths range from 2 to 1250 μs, the latter corresponding to 180 electrical degrees of conduction at 400 c/s. Peak forward current is the dependent variable. The ratings apply for sinusoidally shaped current pulses since this type of pulse is prevalent in applications requiring high-frequency SCRs. Since the circuit designer can normally exercise more control over case temperature than the other parameters, curves were drawn for three values of case temperature which were chosen to cover a practical range of operation. When necessary, as will be shown in the application examples later, the values may be replotted so that interpolation for other values of case temperature may be easily performed.

The notes on the curves specify additional conditions which must be controlled. The reverse voltage during the turn-off time interval must be controlled since it affects the turn-off time value which is a controlled parameter. Device *di/dt* capability is affected by gate drive, and the minimum requirements must be met or exceeded to prevent loss of commutation in inverter cases and, in some cases, possible device destruction.

Power and Energy Curves

In order to choose a suitable heat sink, the circuit designer must be able to determine the power loss in the SCR under his operating conditions. Two curves are provided for this purpose.

One curve is shown in Fig. 4. It gives energy per pulse for sinusoidal current pulses for various values of peak current and pulse base width. This one curve applies for all points of operation depicted on Figs. 1, 2, and 3. To obtain average power dissipation, multiply the energy per pulse value given on the curve by the repetition rate.

For anode current pulse shapes other than sinusoidal, the instantaneous power curve shown in Fig. 5 may be used. Average power dissipation may be arrived at by first plotting the anode current waveform on this graph and then replotting on linear paper the values of instantaneous power vs. time as given by the intersections of the current curve and power curve. The area under the resultant curve gives the energy per anode current pulse, in watt-seconds, which may be then multiplied by the pulse repetition rate to give the average power dissipation.

Gate Circuit Design Requirements

Gate drive affects the switching speed of the SCR during turn-on and this, in turn, affects the *di/dt* capability. In short, low gate drive results in high switching

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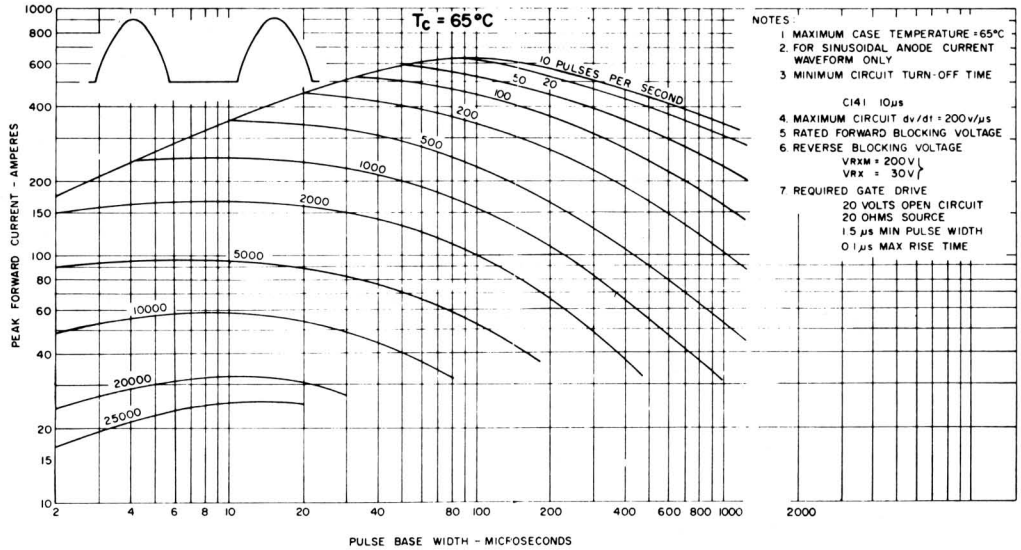


Fig. 1. Peak forward current vs. pulse width, T_c = 65°C.

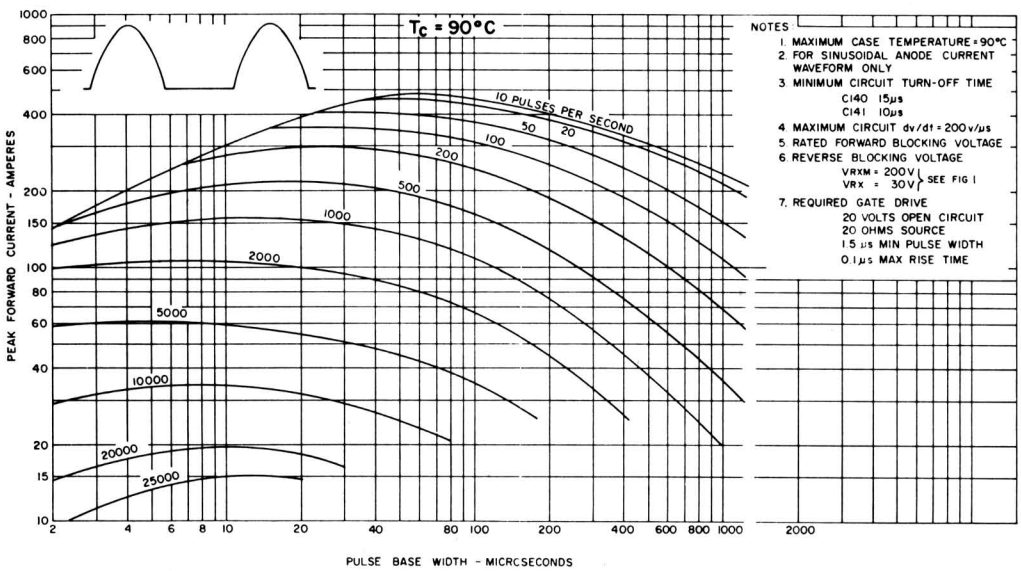


Fig. 2. Peak forward current vs. pulse width, T_c = 90°C.

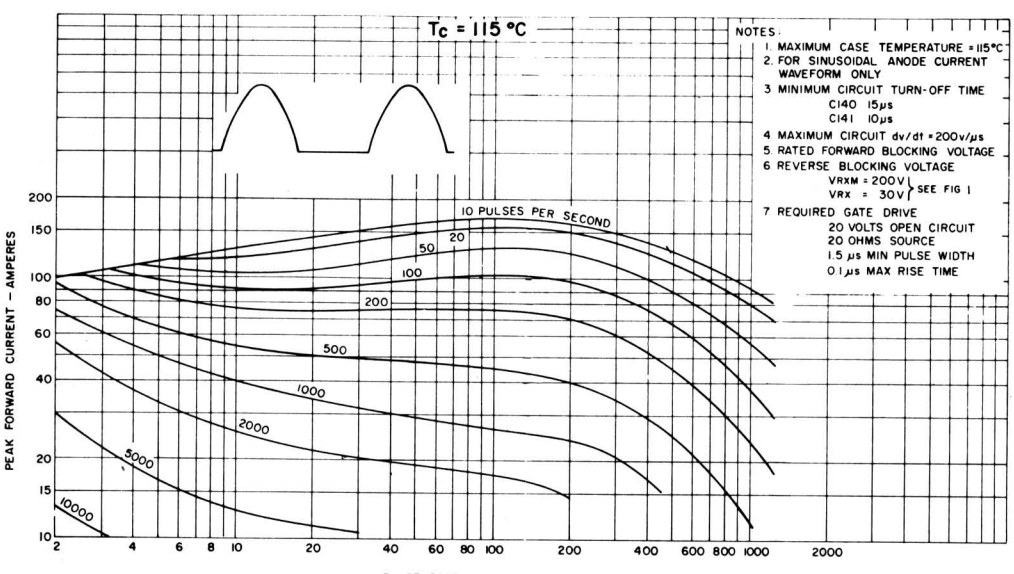


Fig. 3. Peak forward current vs. pulse width, T_c = 115°C.

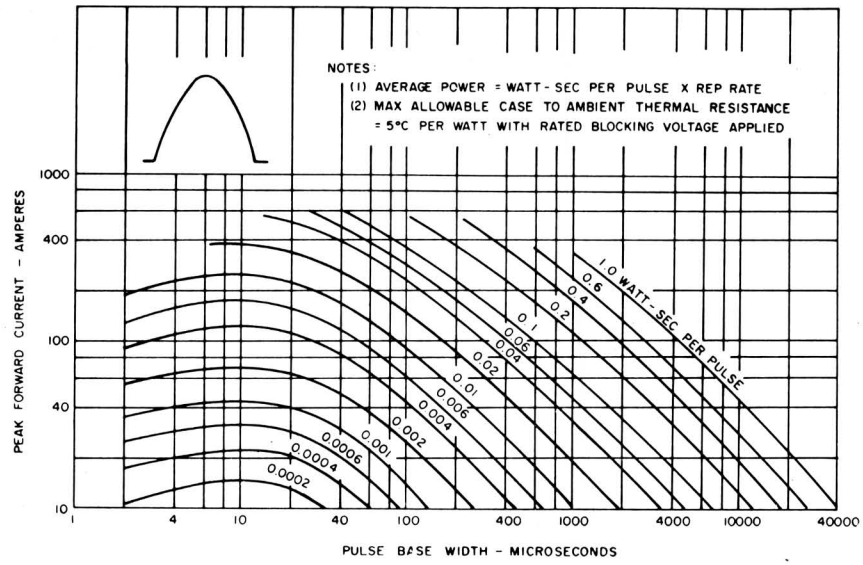


Fig. 4. Energy per pulse for sinusoidal pulses.

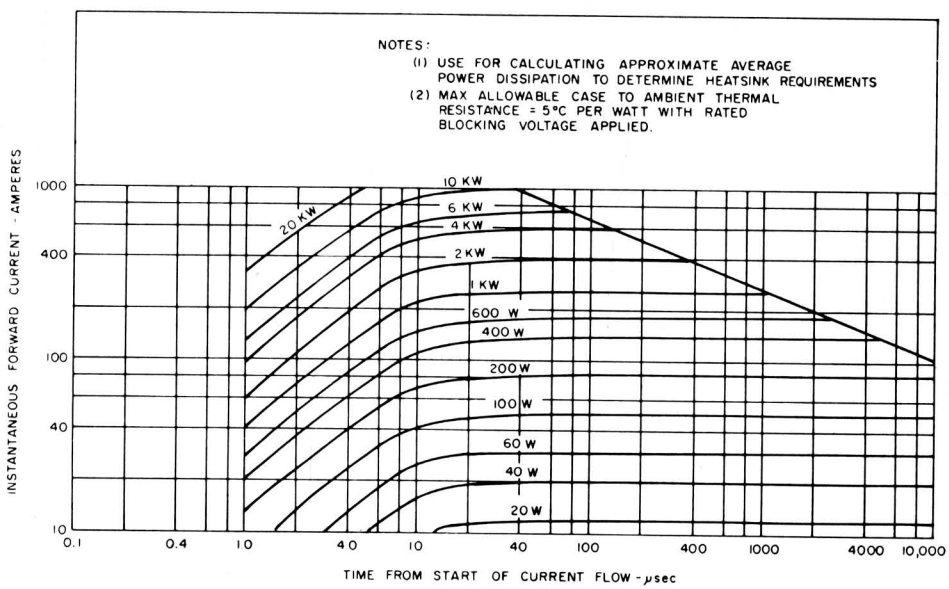


Fig. 5. Instantaneous forward power dissipation.

losses which produce increased SCR heating and poor circuit efficiency. For pulse operation, therefore, it is necessary to adhere to the manufacturer's recommendations for minimum gate drive to achieve satisfactory performance from the high speed SCR.

Figure 6 depicts the range of gate characteristics which exist for one type of SCR. These characteristics vary from device to device and, therefore, the gate driving circuit must be capable of working into a wide range of resistance. An upper limit for instantaneous gate power dissipation also is imposed to prevent device damage.

Figure 6 allows the circuit designer a great deal of flexibility in the design of the triggering circuit. Load lines may be conveniently drawn directly on Fig. 6. It is only necessary that they pass through the shaded area; that is, the instantaneous power limit must not be exceeded and the gate drive must not be lower than the minimum shown when operation at high values of di/dt is planned.

Rectangular Current Pulse Ratings

Figure 7 shows peak current capability vs. allowable case temperature for rectangular current waveforms within the frequency range of 50 to 400 c/s. These curves apply only for cases where switching losses are relatively insignificant, that is, for low values of di/dt. Although it would be more complete to present high-frequency rectangular rating information as was done for the case of sinusoidal pulses, practical techniques for obtaining this information are not fully developed at this time. Conventional rating techniques were employed in the case of the rectangular ratings. As we shall see later, this approach is unsatisfactory when switching losses are significant.

Figure 8 gives average power dissipation for the ratings given in Fig. 7.

Figure 9 gives turn-off time information applicable

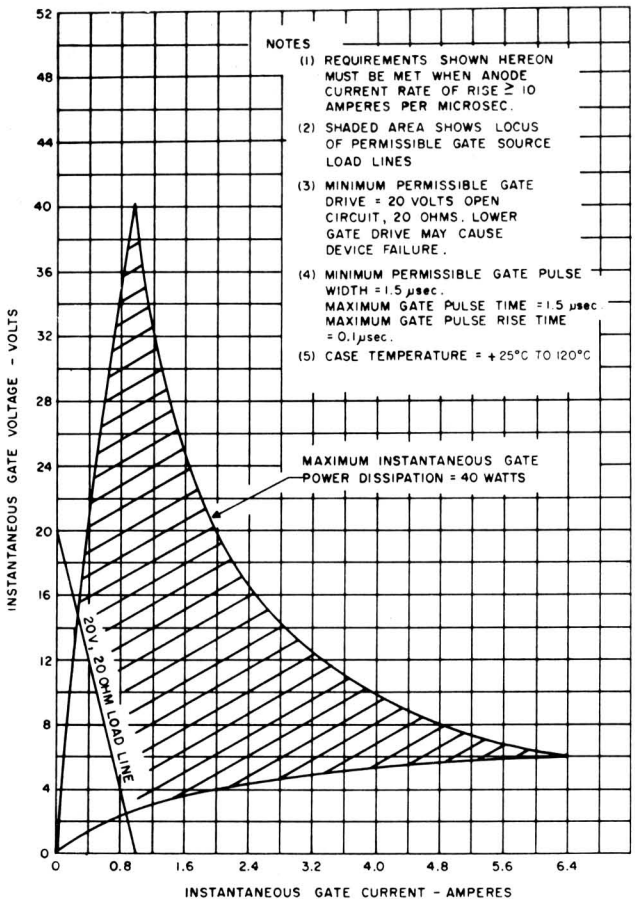


Fig. 6. Gate trigger requirements for high-frequency and high-di/dt operation.

under the conditions of Fig. 7. Note that limit turn-off time under these conditions increases with peak current. This was not the case on the curves for the high-frequency sinusoidal current ratings because the peak current ratings were arrived at through concurrent characterization at a fixed turn-off time.

Use of the Performance Curves

The high-frequency SCR, designed to have high di/dt capability and low switching losses, makes practical many applications which previously imposed operating conditions too severe for the SCR to withstand. In conventional SCRs, high cyclic switching losses are compounded through operation at higher frequencies and they have to be drastically derated to prevent loss of commutation. Many pulse applications, even at low repetition rates, imposed di/dt conditions which would cause instantaneous failure of conventional SCRs. With the availability of high frequency SCRs, however, equipment designers can now apply SCRs to ultrasonic generators, sonar transmitters, high-frequency fluorescent lighting applications, and many others and predict SCR performance in advance through the use of high-frequency performance curves.

The Appendix shows some examples of the use of performance curves to apply the high-frequency SCR to specific operating conditions found in typical applications.

Example I of the Appendix illustrates the case of a sinusoidal current pulse recurring at a 5-kc repetition rate. Since no rating curves are published for 80°C case temperature, interpolation of the available 65, 90, and 115°C curves (Figs. 1, 2, and 3) is necessary. This may be easily done by replotting peak current vs. case temperature for the specific operating conditions specified. In order to determine the requirements for a suitable heat sink, it is first necessary to determine the power loss in the SCR. For the case of sinusoidal current pulses, Fig. 4 may be used. Before the thermal resistance of the required heat sink is calculated, gate and blocking losses must first be added to the forward conduction loss.

Example II of the Appendix involves a low-frequency low-di/dt current pulse. Since the repetition rate is within the 400-c/s limitation, Figs. 7, 8, and 9 may be used to obtain the desired information as shown in the example. Note that, since conventional rating techniques have been employed in this case, the turn-off time value must be determined from Fig. 9 where turn-off time is given as a function of peak forward current.

For the case of a high-frequency rectangular pulse with a high di/dt initial condition, such as shown in Example III, an approximate approach is presented since a rigorous approach has not yet been developed. The general approach taken is explained in the example. The waveform is divided into two portions and their effects are added together to arrive at the maximum allowable case temperature. In this particular case, a conservative answer results. For some cases, however, particularly for the case where the initial pulse is very narrow compared to the rectangular portion, the results using this method may be too optimistic. Further details are given in Example III of the Appendix where the development of ratings for high-frequency irregular anode current pulses is discussed.

Example IV of the Appendix involves another waveform commonly encountered. In this example, the initial pulse is high in amplitude and narrow in base width, and a check must be made to determine if the pulse is within safe operating limits for the SCR as defined on the turn-on current limit curve in Figure 10. It is found to be within rating providing the specified minimum gate drive requirements are adhered to. The 20-volt open-circuit 20-ohm gate drive is a minimum permissible load line for the high di/dt rating. It is definitely recommended that triggering circuits be designed which exceed this minimum.

The example shows how the initial pulse and rectangular portions of the waveform are analyzed to determine the SCR power dissipation. Although the initial pulse is sinusoidal in this example, note that the instantaneous power dissipation curve, Fig. 5, applies for any current waveform.

Since the rectangular portion of the waveform is long in duration compared to the initial pulse, the effect of the initial pulse may be considered simply by adding its average dissipation in the SCR to that which results from the rectangular portion. Thus, the 2900 watts dissipated during the first 40 μs reduces to $2900 \times (40/16\,700) = 7$ watts full cycle average. To this is added the $40 \times (8.3/16.7) = 20$ watts full cycle average for the rectangular

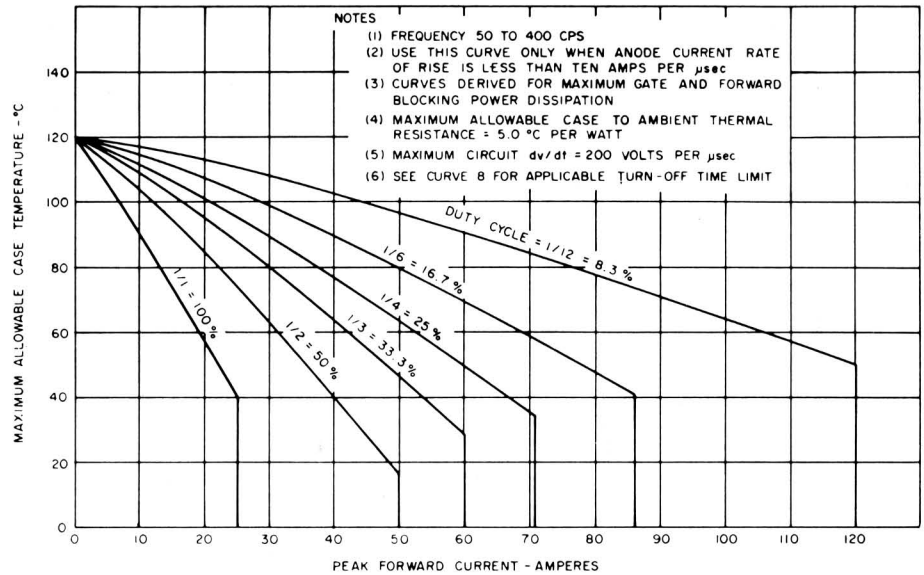


Fig. 7. Case temperature for low-frequency rectangular current waveform.

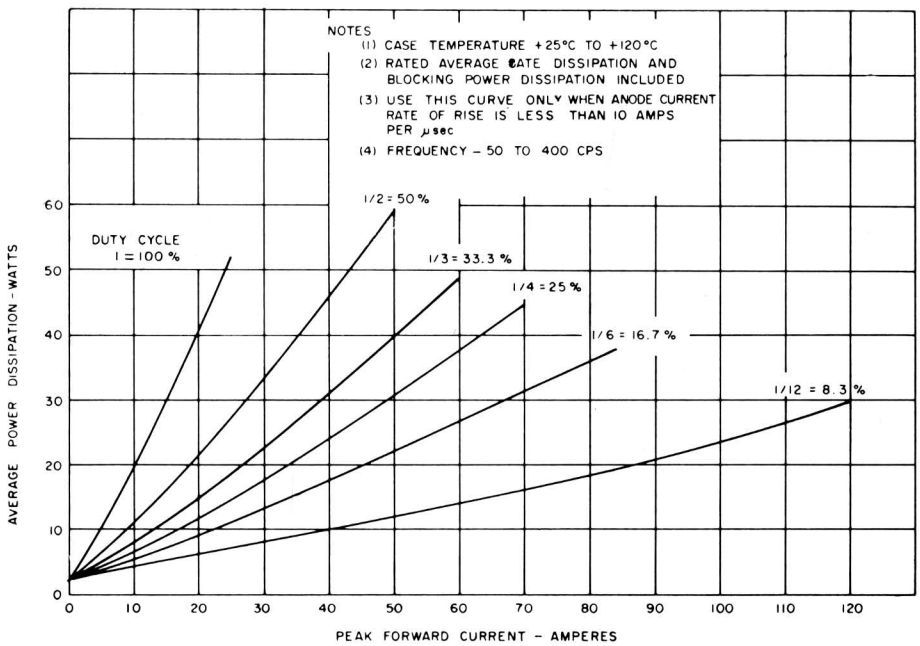


Fig. 8. Average power dissipation for low-frequency rectangular current waveform.

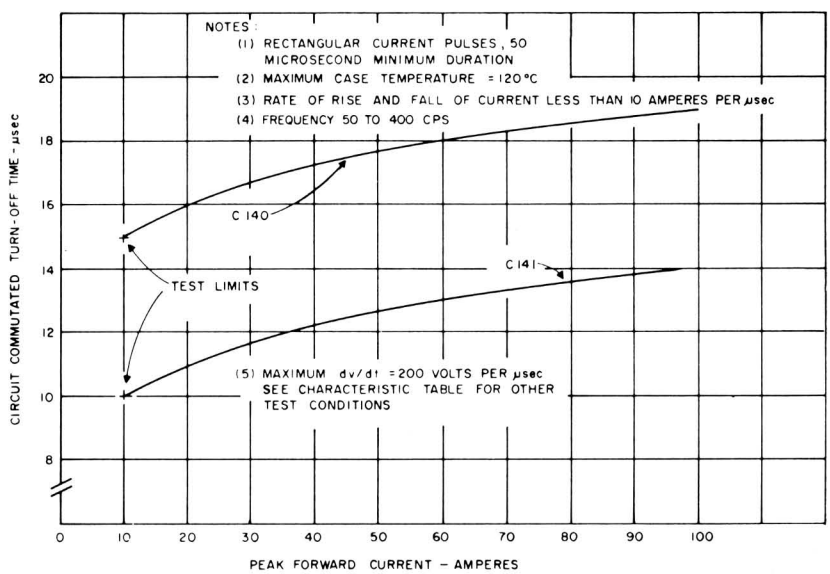
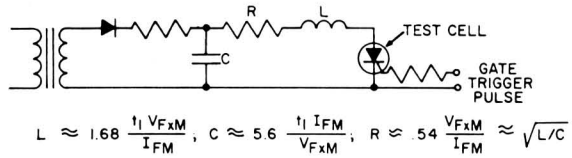
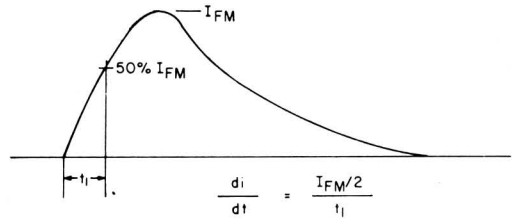


Fig. 9. Conventional turn-off time vs. peak forward current for rectangular current waveform.



$$L \approx 1.68 \frac{t_1 V_{FxM}}{I_{FM}}, \quad C \approx 5.6 \frac{t_1 I_{FM}}{V_{FxM}}, \quad R \approx .54 \frac{V_{FxM}}{I_{FM}} \approx \sqrt{L/C}$$



TEST CONDITIONS

A.	TIME, t_1	$= 1$ μsec.
B.	I_{FM}	_____ AMPERES
C.	PULSE REPETITION RATE	_____ PPS
D.	TEMPERATURE SPECIFY CASE OR AMBIENT	_____ °C
E.	FORWARD BLOCKING VOLTAGE, V_{FxM}	_____ VOLTS
F.	GATE TRIGGER PULSE:	
	1. PULSE WIDTH, t_w	_____ μsec.
	2. RISE TIME, t_r	_____ μsec
	3. OPEN CIRCUIT VOLTAGE	_____ VOLTS
	4. TOTAL SERIES RESISTANCE	_____ OHMS

Fig. 10. Waveform and conditions for *di/dt* test.

portion. The allowable case temperature is then arrived at by considering the total power dissipation as being the result of a purely rectangular waveform.

In this case the frequency is 60 c/s, which is within the range of Figs. 7 and 8. For frequencies above 400 c/s, the discussion of Example III is applicable. Frequencies below 50 c/s result in high cyclic temperature excursions within the SCR, and a different rating approach becomes necessary [2].

Rating the High-Frequency SCR

The considerations and techniques employed in rating high-frequency SCRs are necessarily different from those which have been previously employed for conventional 50- to 400-c/s devices. In order for an SCR to perform well at high frequencies, it must be specifically designed for this type of operation. Otherwise ratings would be too low to make widespread use of the device practical.

Design Considerations

Although it is not the purpose of this paper to discuss device design in detail, a brief discussion of some of the more important considerations and resultant limitations will be included to provide the circuit designer with answers to some questions which might arise when considering the high-frequency SCR for his application.

In order to make an SCR which will perform satisfactorily under operating conditions where high *di/dt*, high *dv/dt*, and short turn-off time are all desirable, a delicate balance must be maintained among several factors.

In order to have high *dv/dt* capability, a short-circuited emitter design is employed which prevents the capacitive current through the *p-n-p-n* device junctions from reaching the switching point during the application of a fast rising voltage wavefront. Some of this current is bypassed around one of the junctions through the shorted emitter [3].

Short turn-off time is accomplished through control of the silicon lifetime which is a measure of how quickly the charged carriers in the device recombine and become neutralized. The device cannot block reapplied forward blocking voltage until such time as this neutralization is effected. Lifetime control is achieved through the diffusion of gold into the silicon pellet.

High *di/dt* capability is primarily achieved through fast turn-on within the first microsecond. The conventional SCR turns on first in a small fraction of the pellet area near the gate lead. This area then propagates with time, the rate of which depends somewhat on lifetime as did turn-off time. In a high-frequency SCR, a distributed gate area is used to enlarge the initial area of turn-on; this reduces the power generated by the rising current and decaying voltage.

Control of the above mentioned items is a compromise. Device lifetime affects both *di/dt* and turn-off time but in opposite directions. Emitter short circuiting increases *dv/dt* capability but, in turn, raises gate trigger currents. Gold diffusion increases high temperature blocking currents significantly, thereby reducing blocking voltage ratings, and also increases forward on-voltage. Thus, a trade off is encountered when trying to optimize devices which have the combination of short turn-off time, good *di/dt*, and high blocking voltage capability; the best balance possible must be achieved to meet the ultimate application.

di/dt Testing

Since an SCR cannot switch instantaneously from the blocking state to the conducting state, the instantaneous product of the decaying blocking voltage and the rising anode current represents power loss during switching. These losses can easily result in peak powers of several kilowatts when the rate of rise of anode current is sufficiently high. The problem is further compounded by the fact that the entire device junction area is not conducting during switching. This is discussed further in a later section of the paper.

Excessive power dissipation within the device during switching can result in device destruction. Therefore, a device must have a *di/dt* rating established by the manufacturer to enable the circuit designer to design within safe limits.

Figure 10 shows the basic circuit and current waveform normally employed for *di/dt* testing. This method of test is in the process of being adopted by JEDEC as a standard test method. The waveform is produced from a damped *RLC* series circuit with the *R*, *L*, and *C* values selected according to the equations shown on the figure. This results in a near-linear current rise during the time t_1.

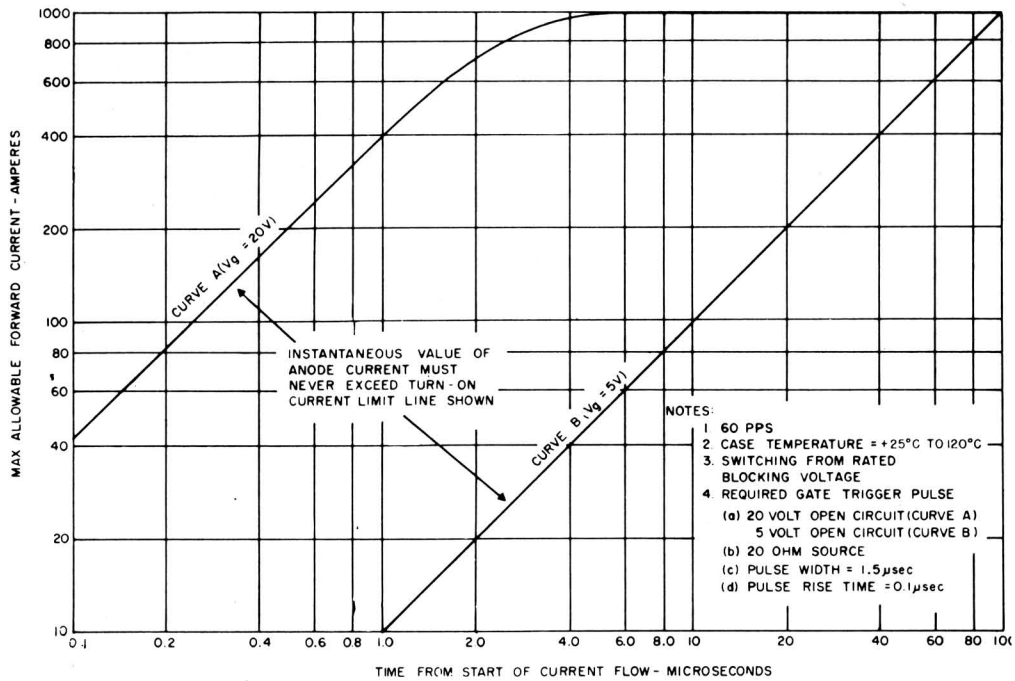


Fig. 11. Turn-on current limit.

The di/dt value is defined as one half the peak current divided by t_1, which is not to be less than 1 μs. Since di/dt failure, if it occurs, will occur within the first microsecond, the current vs. time relationship beyond that point is actually of little consequence.

The important conditions which must be controlled are listed beneath the waveform on Fig. 10. The blocking voltage level is important, since it affects switching power. The gate trigger signal has a pronounced effect on di/dt, since it affects the size of the initial junction area and, thus, the power handling capability.

Many devices must be tested over the operating temperature range to determine the di/dt rating. The results are then shown in the form of the turn-on current limit curve in Fig. 11.

The second curve shown on Fig. 11, depicts a much lower di/dt limit for cases when gate drive is reduced. This is included primarily to alert the circuit designer to the fact that di/dt capability is dependent on gate drive. Thus, care must be taken in the application of the device that no low energy or noise signals be allowed to trigger the SCR in circuits where high anode current rates of rise exist.

Concurrent Characterization

The subject of concurrent characterization of the important device dynamic characteristics, dv/dt, turn-off time, and di/dt, is discussed in detail in another paper [1]. However, since this technique is the basis for the generation of high-frequency ratings, a brief summary is included here.

When SCRs are subjected to current pulses with rates of rise in the tens to hundreds of amperes per microsecond range, incomplete utilization of the device junction area may result, although the operating point may be considerably below the value shown on the turn-on current limit curve. The conventional device will normally turn-on in a small area physically near the gate which will grow in size with time until the entire cathode emitter area becomes effective. Since this propagation takes in the order of 10 to 100 μs, depending on the design of the particular device as well as the application conditions, it is not uncommon for only a fraction of the junction area to be effective in many pulse applications.

Figure 12 illustrates typical conventional designs where, during a pulse of anode current, only a fraction of the junction area becomes conductive. The small current-carrying area results in increased on-voltage (forward voltage drop). Consequently, losses are increased which result in higher junction temperatures.

Both turn-off time and dv/dt capability decrease with increasing junction temperature. Therefore, the presence of hot spots resulting from localized heating may cause circuit malfunction even though the specified value of any one of the three important dynamic characteristics was not exceeded from the standpoint of individual characterization. Thus, the need for concurrent characterization becomes apparent.

The method used to perform concurrent characterization is the pulse turn-off time test [1]. The waveforms employed are shown in Fig. 13. This test is extremely effective in detecting the presence of junction hot-spots since they are accounted for by loss of commutation when the device is too hot to block forward voltage following a pulse of forward current.

Derivation of High-Frequency Performance Curves

Application of the pulse operation test over a wide range of pulse base widths, repetition rates, peak currents, and case temperatures results in rating curves of the type

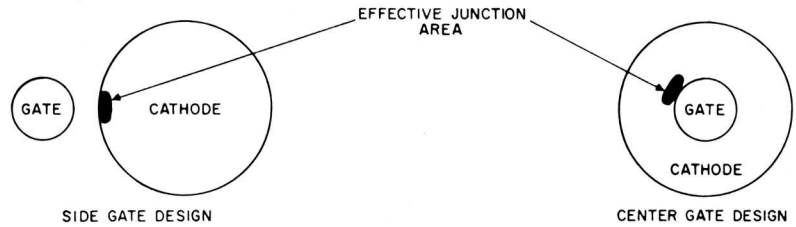


Fig. 12. Illustrations of reduced junction area which may occur in some SCRs during turn-on of fast-rising current pulses.

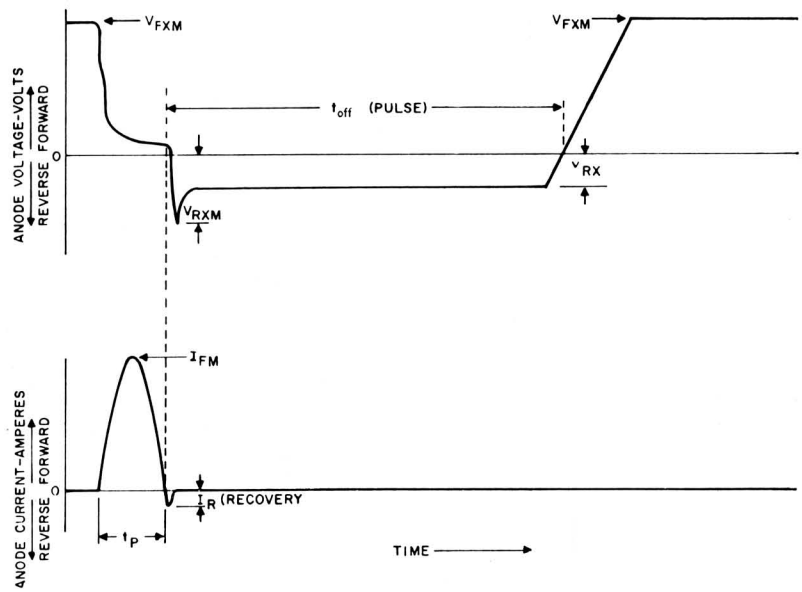


Fig. 13. Current and voltage waveforms for pulse operation turn-off time test.

shown in Figs. 1, 2, and 3. Since concurrent characterization is employed, all points shown apply for controlled values of *di/dt*, *dv/dt*, and turn-off time. At the wider values of pulse base width, switching losses are quite negligible since the *di/dt* of anode current is low. A computer, using previously developed rating techniques, was employed to develop these portions of the curves. At the shorter pulse base widths where the entire junction area is not effective and the *di/dt* is relatively high, the curves were developed through the use of concurrent characterization. Analytical techniques for the generation of these data are presently being finalized.

Although many alternatives existed for the presentation of the rating curves, the method chosen was felt to be the most flexible. The values of turn-off time and *dv/dt* are held constant at their factory tested values. Although allowing a longer turn-off time would result in higher peak forward current without loss of commutation, this practice results in higher peak junction temperatures. In the interests of long-term device stability, it was felt that higher peak junction temperatures should be avoided. It was also felt that a constant turn-off time value was more realistic from the application standpoint. The curves may be used for circuits where the available turn-off time is longer, but no increase in current is permitted over the value given by the curves for the limit turn-off time case.

Frequency is shown as a parameter on the curves. Using a logarithmic scale, it is a simple task to interpolate for intermediate frequencies.

di/dt Capability vs. High-Frequency Ratings

The values of *di/dt* that exist for all points shown on Figs. 1, 2, and 3 are considerably lower than that shown on the turn-on current limit curve in Fig. 11. As mentioned previously, Fig. 11 shows device capability to withstand high *di/dt* without damage. The device *is not required to commutate under these conditions*, while in Figs. 1, 2, and 3 the device will commutate off within the specified turn-off time following the anode current pulse. The reduction of peak current to values considerably below those permitted by the turn-on current limit curve is necessary to control the device junction temperature to values which will allow the device to turn off during the specified time interval.

Comparison of Rating Methods

Conventional SCR Ratings

Until recently, SCRs were designed and rated primarily for low-frequency phase controlled applications. The rating system generally used is based on maintaining constant peak junction temperature [4]. The rated junction temperature of the device is not exceeded at any point during the cycle of operation with this system.

The basic ratings consist of average forward current vs. maximum allowable case temperature curves for various conduction angles of a 50- to 400-c/s phase controlled sinusoidal current waveform. The method of calculation consists of determining the peak junction

temperature rise above the case and then subtracting this rise from the maximum permitted junction temperature to obtain the maximum allowable case temperature.

The junction temperature rise is calculated using the basic relationship ΔT = Power $\times$ thermal resistance together with the principle of superposition [2]. The power is obtainable from the on-voltage curve of the particular device. The thermal resistance value is the transient thermal impedance of the device which accounts for the thermal response as a function of time. Both the on-voltage and the thermal impedance are functions of the device junction area.

At frequencies below 50 c/s, the longer cycle time allows the device junction temperature to follow the applied waveform more closely, since the thermal time constant is more closely approached. This results in higher junction temperature excursions which, if peak junction temperature is fixed, means that lower case temperature ratings are necessary. At frequencies above 400 c/s switching losses begin contributing significantly to the junction temperature rise. Switching losses are not included in the rating system since they are extremely difficult to express analytically for reasons to be explained in the following section of the text.

High-Frequency Ratings

The methods used for developing ratings on conventional SCRs cannot be used for high-frequency SCRs since switching losses definitely must be considered. The problem is further complicated by the fact that, under conditions of short pulse operation, the entire junction area may not be conducting.

The fact that the effective junction area is time dependent creates major problems in determining the on-voltage and thermal impedance values normally used in rating calculations. This on-voltage is not only time dependent, but also depends on the initial blocking voltage level and the magnitude of the applied gate trigger signal. The thermal impedance is difficult to calculate and even more difficult to measure in the microsecond time range.

Consequently, peak junction temperature cannot be readily determined under conditions of pulse operation and a different approach to rating is necessary. Following commutation the device will be required to block rated voltage. Therefore, it is only necessary to control the junction temperature at the end of the turn-off time interval. Concurrent characterization through the pulse turn-off time test provides a means of ensuring this. The effects of increased switching losses at high frequencies are also considered by this approach.

Pulse Operation Life Tests

Conventional life tests are not realistic indicators of performance for high-frequency SCRs. A device which is expected to operate under conditions of pulse operation should definitely be life tested in that manner. Of primary concern is the effect that the high peak junction temperatures encountered might have on long-term stability; 1000-hour pulse operation life tests have been performed as a check on the high-frequency performance curves shown with no measurable degradation of characteristics.

Inverter Type SCRs

Presently several types of conventional SCRs are classified as inverter types, since they are specially selected for specific values of turn-off time. At high frequencies or where high values of *di/dt* exist and switching losses are significant, these types often fail to work even though the circuit designer has carefully provided the required turn-off specified by the manufacturer. For these applications, a high-frequency SCR rated by using concurrent characterization is the solution. Turn-off time selection alone is not sufficient to ensure satisfactory circuit operation.

High-Frequency SCRs Available

The performance curves included in this paper apply to the General Electric C140 and C141 types (2N3649 through 2N3658) which have been specifically designed for high-frequency operation. The C140 and C141 differ only in turn-off time. The C140 turn-off time is 15 μs under pulse conditions, whereas the C141 turn-off time is 10 μs. Both types are rated to handle 25 amperes dc.

Conclusion

The high-frequency SCR is adaptable to many applications which previously imposed dynamic conditions too severe for SCRs to withstand. High-frequency performance curves, based on concurrent characterization of the important dynamic characteristics, allow the circuit designer to predict performance of the SCR in his circuit with confidence.

Appendix

Example I: High-Frequency Sinusoidal Pulse

Problem: Find the maximum allowable average anode current that can be carried by a C141 if the pulse is 50 μs wide and the repetition rate is 5000 c/s. The case is held at 80°C. What is the dissipation in the SCR? Find the maximum permitted thermal resistance between case and cooling air at 45°C. Assume the gate and blocking losses total 1 watt.

Answer: From Fig. 1 (65°C) the maximum permitted peak current at 5000 c/s, 50 μs pulse width is 72 amperes; Fig. 2 (90°C), 45 amperes; Fig. 3 (115°C), 10 amperes. Interpolation gives the permitted peak current at 80°C as 55 amperes peak.

$$\text{average current} = I_{pk} \times \frac{2}{\pi} \times \frac{\text{pulse width}}{\text{pulse period}}$$

$$= 55 \times \frac{2}{\pi} \times \frac{50}{200}$$

$$= 8.8 \text{ ampere average.}$$

From Fig. 4 at 50 μs pulse width and 55 amperes peak current, the energy dissipated per pulse is 0.003 W·s per

pulse. The average anode dissipation is 0.003 × 5000 = 15 watts.

From this information, the heatsink can be chosen using the equation:

maximum case to cooling fluid thermal resistance

$$= \frac{\text{case temperature} - \text{cooling fluid temperature}}{\text{anode dissipation} + \text{gate \& blocking losses}}$$

$$= \frac{80 - 45}{15 + 1} = 2.2°\text{C/W}.$$

Note that a turn-off of 10 μs and a dv/dt at 200 V/μs can be applied concurrently to the C141 at the above current and temperature conditions.

Example II: (Low-Frequency Low-di/dt Pulse)

Problem: A C140 is carrying a 20-ampere rectangular pulse, 833 μs wide at a repetition rate of 400 pps. The initial di/dt is 5 amperes per μs. What is the maximum allowable case temperature? What is the power dissipation? What turn-off time and dv/dt may be applied to the C140?

Answer: An 833-μs pulse in a 2.5-ms period gives a duty cycle of

$$\frac{833}{2500} \times 100 = 30 \text{ percent}.$$

Figure 7 shows that, with this duty cycle, a 20-ampere rectangular pulse has a maximum allowable case temperature of 98°C. Figure 8 gives the total dissipation as 13.5 watts.

From Fig. 9, 20 amperes forward current permits a turn-off time of 16 μs and a dv/dt of 200 V/μs to be applied concurrently.

Example III: High-Frequency Irregular Pulses

Problem: What is the maximum allowable case temperature for a C141 carrying the anode current waveform shown in Fig. 14? What turn-off time and dv/dt may be applied?

Answer: No rigorous method has yet been developed for handling this case. The following method is approximate only but provides a conservative answer.

The di/dt of the initial pulse imposes the most severe strain on the SCR during the cycle. Use the initial half-cycle to establish a case temperature, and then lower the case temperature by an amount equal to the effective thermal resistance (dc) of the SCR multiplied by wattage dissipated during the rest of the cycle (t_1 to t_2) to establish the maximum permitted case temperature.

The average anode dissipation (time t_1 to t_2) can be found by means of Fig. 5 (for method see Example IV). The energy dissipated per pulse is 0.0032 W·s. The average anode dissipation = 0.0032 W·s × 5000 pps = 16 watts.

Figure 2 shows that a 5000-cycle 50-ampere 20-μs pulse allows a case temperature slightly higher than 90°C. Substract from this case temperature a temperature of

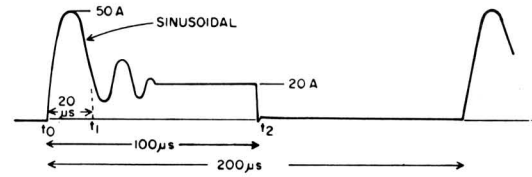


Fig. 14. Current waveform for Example III.

1.7°C/W × 16 watts = 27°C to give the maximum permitted case temperature, with the given waveform, of 90°C − 27°C = 63°C. As the end of the current pulse is rectangular, Fig. 9 will have to be used to find the required turn-off time which is 16 μs. The concurrent dv/dt is 200 V/μs.

Actually, in this case the effects of the initial pulse are essentially negligible at the 100-μs point. The case temperature value of 90°C obtained from Fig. 2, considering the initial pulse alone, applies for the turn-off time value stated on that figure. This means that the junction temperature has, at that time, cooled back down to approximately its steady state value.

The additional reduction in case temperature from 90 to 63°C to allow for the presence of the rectangular portion of the current waveform considers the average temperature rise of the junction above the case. It would be better to consider the peak temperature rise rather than the average, but it makes little difference in this case, since the device is essentially all turned on near the start of the rectangular portion. This is determined by noting the time at which the power curves on Fig. 5 flatten out. With the device area all turned on, the peak junction temperature rise above the average value will be very slight for a 80-μs pulse width since the transient thermal impedance value will be quite low.

For cases where the junction area does not become entirely turned on, the approach used in this example will under some conditions produce results which are optimistic. This is generally true when the rectangular portion of the pulse occurs prior to the time the entire junction area turns on. This can result in high junction temperature cycling above the average value. It is best to consult the device manufacturer for his recommendations in this case.

Example IV: Low-Frequency Irregular Pulses With High Initial di/dt

Problem: What is the maximum allowable case temperature for a C141 carrying the anode current waveform shown in Fig. 15?

Answer: Check the initial di/dt by plotting the first 10 μs of current flow on Fig. 11. The waveform is found to be within safe limits provided that the high gate pulse shown on Fig. 6 is used. Note that an inadequate gate pulse could destroy the SCR. To find the anode dissipation, plot the anode current waveform on Fig. 5 as shown in Fig. 16.

Replot the intersections of anode current with the instantaneous power lines. In this case, it is convenient

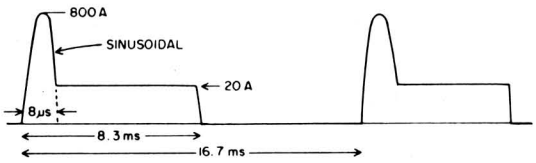


Fig. 15. Current waveform for Example IV.

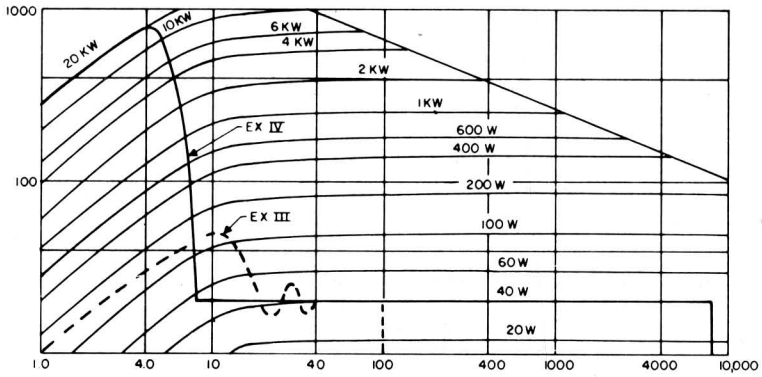


Fig. 16. Determination of anode power dissipation for Example IV.

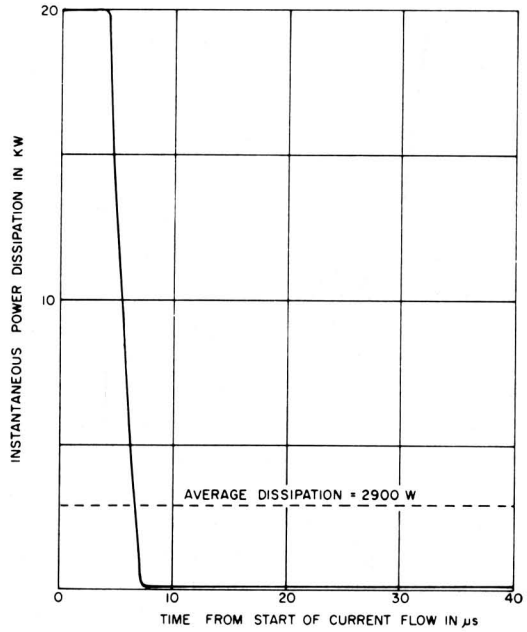


Fig. 17. Instantaneous anode power dissipation replot for Example IV.

to replot the first 40 μs of current flow separately in order to use a convenient scale. This is shown in Fig. 17.

By graphical integration, the energy per pulse for the first 40 μs is seen to be 0.12 W s. To this must be added the energy dissipated during the rectangular portion of the pulse which is 40 watts × 8.3 ms = 0.33 W·s.

Thus, the total energy dissipated per pulse is 0.12 + 0.33 = 0.45 W·s. The average dissipation due to anode current flow is 0.45 W·s × 60 pps = 27 watts.

As the repetition rate is within the limits of 50 to 400 c/s, a convenient way of ascertaining the maximum permitted case temperature is to convert the high di/dt irregular waveform to a low di/dt rectangular pulse with the same dissipation.

From Fig. 8, a 27-watt 50-percent duty cycle pulse gives an average anode current of 25 amperes peak.

From Fig. 7, a 25-ampere 50-percent duty cycle current gives a maximum allowable case temperature of 75°C.

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